



St. MARTIN'S ENGINEERING COLLEGE

UGC Autonomous

NBA & NAAC A+ Accredited

Dhulapally, Secunderabad – 500100



Department of Electronics & Communication Engineering

TIME - TABLE

Year : II B.Tech

Semester : I

Section : A

Academic Year : 2023-24

Room No : 1322

Block Name : MG Block

W.e.f : 04-10-2023

Class In charge : K Balasubramanyam

HOUR	9:20 AM to 10:10 AM	10:10 AM to 11:00 AM	11:00 AM to 11:50 AM	11:50 AM to 12:40 PM	LUNCH BREAK			1:20 PM to 2:10 PM	2:10 PM to 3:00 PM	3:00 PM to 3:50 PM
DAY	1	2	3	4	5	6	7	BS(B1)/DLD (B2) GRR,AS/NS, BA		
MON	S&S GRR	NMCV MSR	DLD SKS	NAS PP						
TUE	DLD SKS	NMCV MSR	NAS PP	S&S GRR				NMCV MSR	S&S GRR	LIB/SPT KB
WED	NAS PP	AC(B2)/DLD (B1) KB, JR/NS, BA						CA CS	AC KB	DLD SKS
THU	AC KB	COI MP	S&S GRR	AC KB				NAS PP	APT KRI	COI MP
FRI	NMCV MSR	AC KB	NAS PP	DLD SKS				S&S GRR	SK AS	COI MP
SAT	DLD SKS	BS(B2)/AC(B1) GRR,AS/KB, JR						NMCV MSR	AC KB	MMM

- NMCV : Numerical Methods and Complex Variables
- AC : Analog Circuits
- NAS : Network Analysis and Synthesis
- DLD : Digital Logic Design
- S&S : Signals and Systems
- AC LAB : Analog Circuits Laboratory
- DLD LAB : Digital logic Design Laboratory
- BS LAB : Basic Simulation Laboratory
- COI : Constitution of India
- SK : Soft Skills
- APT : Aptitude
- CA : Club Activity
- LIB/SPT : Library / Sports
- MMM : Mentor Mentee

- MSR : M SANDHYA RANI
- KB : K BALASUBRAMANYAM
- PP : P PRIYANKA
- SKS : Dr SANJAY KUMAR SUMAN
- GRR : G RAMESH REDDY
- KB, JR : K BALASUBRAMANYAM, J RAMESH
- NS, BA : N SOWMYA, B ANUSHA
- GRR, AS : G RAMESH REDDY, CH ANUSHA
- MP : M PRATHUSHA
- AS : Ch ANUSHA
- KRI : K RAJESHWARI
- CS : C SRIDEVI
- KB : K BALASUBRAMANYAM

 18/09/23	 18/9/23		 19/9/23
CHIEF IN CHARGE (TIME TABLES)	HOD-ECE	PRINCIPAL	GROUP DIRECTOR

Head of the Department
 Department of Electronics & Communication Engineering
 St. Martin's Engineering College
 Dhulapally, Secunderabad, Telangana-500100

18/09/23
 GROUP DIRECTOR
 ST. MARTIN'S ENGINEERING COLLEGE
 UGC - AUTONOMOUS
 Survey No. 98 & 100, Dhulapally (V),
 Dundigal, Gandimaisamma (M), Medchal-Malkajgiri (I)
 Dhulapally, Secunderabad-500 100, Telangana.



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Department of Electronics & Communication Engineering

TIME - TABLE

Year : II B.Tech

Semester : I

Section : B

Academic Year : 2023-24

Room No : 1320

Block Name : MG Block

W.e.f : 04-10-2023

Class In charge : L Chandra Shekar

HOUR	9:20 AM to 10:10 AM	10:10 AM to 11:00 AM	11:00 AM to 11:50 AM	11:50 AM to 12:40 PM	LUNCH BREAK			1:20 PM to 2:10 PM	2:10 PM to 3:00 PM	3:00 PM to 3:50 PM
DAY	1	2	3	4	5	6	7			
MON	NAS PP	COI MP	NAS PP	S&S AS	L N U N C H B R E A K	NMCV MSR	AC LCS	S&S AS		
TUE	AC LCS	S&S AS	NMCV MSR	SK CS		NAS PP	DLD GUS	LIB/SPT LCS		
WED	S&S AS	NMCV MSR	AC LCS	COI MP		AC (B1)/BS (B2) LCS,GP/AS,NBR				
THU	DLD GUS	BS (B1)/DLD (B2) AS,NBR/KK,PK				AC LCS	APT KD	DLD GUS.		
FRI	S&S AS	AC (B2)/DLD (B1) LCS,GP/KK,PK				NMCV MSR	NAS PP	CA SR		
SAT	NMCV MSR	NAS PP	DLD GUS	COI MP		DLD GUS	AC LCS	MMM		

NMCV : Numerical Methods and Complex Variables	MSR : M SANDHYA RANI
AC : Analog Circuits	LCS : L CHANDRA SHEKAR
NAS : Network Analysis and Synthesis	PP : P PRIYANKA
DLD : Digital Logic Design	GUS : G UDAYA SRI
S&S : Signals and Systems	AS : Ch ANUSHA
AC LAB : Analog Circuits Laboratory	LCS : L CHANDRA SHEKAR, G POSHAMALLU
DLDLAB : Digital logic Design Laboratory	KK,PK : K KUMARI, P KIRANMAYEE
BS LAB : Basic Simulation Laboratory	AS,NBR : Ch ANUSHA, G NAVA BHARATH REDDY
COI : Constitution of India	MP : M PRATHUSHA
SK : Soft Skills	CS : C SRIDEVI
APT : Aptitude	KD : K DHARANI
CA : Club Activity	SR : S RAJESH
LIB/SPT : Library / Sports	LCS : L CHANDRA SHEKAR
MMM : Mentor Mentee	

 CHIEF IN CHARGE (TIME TABLES)	 HOD-ECE	 PRINCIPAL	 GROUP DIRECTOR
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GROUP DIRECTOR
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Department of Electronics & Communication Engineering

TIME – TABLE

Year : **II B.Tech** Semester : **I**
 Section : **C** Academic Year : **2023-24**
 Room No : **1319** Block Name : **MG Block**
 W.e.f : **04-10-2023** Class Incharge : **C Sridevi**

HOUR	9:20 AM to 10:10 AM	10:10 AM to 11:00 AM	11:00 AM to 11:50 AM	11:50 AM to 12:40 PM	L U N C H B R E A K	1:20 PM to 2:10 PM	2:10 PM to 3:00 PM	3:00 PM to 3:50 PM
DAY	1	2	3	4		5	6	7
MON	AC CS	AC (B1)/DLD (B2) JR,BA/SPM,GSK				S&S DT	NMCV MSR	COI MP
TUE	DLD SPM	AC (B2)/BS (B1) JR,BA/DT,KNV				NAS CN	AC CS	NMCV MSR
WED	NMCV MSR	DLD SPM	AC CS	S&S DT		COI MP	S&S DT	LIB/SPT CS
THU	S&S DT	NAS CN	COI MP	NAS CN		DLD SPM	AC CS	SK GVU
FRI	NAS CN	NMCV MSR	DLD SPM	CA KR		NAS CN	S&S DT	AC CS
SAT	AC CS	APT LCS	NMCV MSR	DLD SPM		BS (B2)/DLD (B1) DT,KNV/SPM,GSK		MMM

NMCV : Numerical Methods and Complex Variables	MSR : M SANDHYA RANI
AC : Analog Circuits	CS : C SRIDEVI
NAS : Network Analysis and Synthesis	CN : Ch NIROSHA
DLD : Digital Logic Design	SPM : S P MANIKANTA
S&S : Signals and Systems	DT : D THIRUPATHI
AC LAB : Analog Circuits Laboratory	JR,BA : J RAMESH, B ANUSHA
DLD LAB : Digital Logic Design Laboratory	SPM,GSK : S P MANIKANTA/ G SHIVA KUMARI
BS LAB : Basic Simulation Laboratory	DT, KNV : D THIRUPATHI/K N V RAO
COI : Constitution of India	MP : M PRATHUSHA
SK : Soft Skills	GVU : G V UJWALA
APT : Aptitude	LCS : L CHANDRA SHEKAR
CA : Club Activity	KR : K RAJESHWAR
LIB/SPT : Library / Sports	CS : C SRIDEVI
MMM : Mentor Mentee	

 A. V. Jayaram 18/09/23 CHIEF IN CHARGE (TIME TABLES)	 18/9/23 HOD-ECE	 PRINCIPAL	 19/9/23 GROUP DIRECTOR
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Department of Electronics & Communication Engineering

TIME – TABLE

Year : **II B.Tech** Semester : **I**
 Section : **D** Academic Year : **2023-24**
 Room No : **1315** Block Name : **MG Block**
 W.e.f : **04-09-2023** Class Incharge : **G V Ujwala**

HOUR	9:20 AM to 10:10 AM	10:10 AM to 11:00 AM	11:00 AM to 11:50 AM	11:50 AM to 12:40 PM	L U N C H	1:20 PM to 2:10 PM	2:10 PM to 3:00 PM	3:00 PM to 3:50 PM
DAY	1	2	3	4		5	6	7
MON	AC SAR	S&S NV	NMCV MSR	COI MP	B R E A K	DLD GVU	S&S NV	AC SAR
TUE	NAS CN	S&S NV	COI MP	NAS CN		BS (B1)/DLD (B2) NV, KK/GVU, KD		
WED	S&S NV	NAS CN	DLD GVU	AC SAR		NMCV MSR	COI MP	LIB/SPT GVU
THU	NMCV MSR	SK KD	NMCV MSR	DLD GVU		AC (B1)/BS (B2) SAR, KNV/NV, KK		
FRI	DLD GVU	NAS CN	CA DT	NMCV MSR		AC (B2)/DLD (B1) SAR, KNV/GVU, KD		
SAT	AC SAR	NAS CN	DLD GVU	APT BA		S&S NV	AC SAR	MMM

NMCV : Numerical Methods and Complex Variables	MSR : M SANDYA RANI
AC : Analog Circuits	SAR : SUNITA ARVAIND RATHOD
NAS : Network Analysis and Synthesis	CN : Ch NIROSHA
DLD : Digital Logic Design	GVU : G V UJWALA
S&S : Signals and Systems	NV : N VISHWANATH
AC LAB : Analog Circuits Laboratory	SAR,KNV : SUNITHA ARVIND RATHOD, K N V RAO
DLD LAB : Digital Logic Design Laboratory	GVU, KD : G V UJWALA, K DHARANI
BS LAB : Basic Simulation Laboratory	NV, KK : N VISHWANATH, K KUMARI
COI : Constitution of India	MP : M PRATHUSHA
SK : Soft Skills	KD : K DHARANI
APT : Aptitude	BA : B ANUSHA
CA : Club Activity	DT : D THIRUPATHI
LIB/SPT : Library / Sports	GVU : G V UJWALA
MMM : Mentor Mentee	

 A. V. Venkatesh Kumar 18/09/23 CHIEF IN CHARGE (TIME TABLES)	 18/09/23 HOD-ECE	 18/09/23 PRINCIPAL	 19/09/23 GROUP DIRECTOR
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